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Integrated Circuit Design for Miniature Implantable Medical Devices

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Introduction

A new generation of Miniature Implantable Medical Devices (MIMDs) has arrived. Thanks to advances in micro-electro-mechanical systems (MEMS), electronics packaging, and battery technologies, coupled with some creative integrated circuit (IC) design, these new devices are a fraction of the size of traditional Implantable Medical Devices (IMDs).

Traditional IMDs

A traditional IMD consists of a metal case located in the chest or abdomen, and electrical leads connecting the electronics in the case to the point of therapy in the heart, spine, neck, head, or limbs. Examples of these devices include; cardiac pacemakers and defibrillators that perform electrocardiogram (ECG) measurements and electrically stimulate the heart, neuro-stimulators that electrically stimulate the brain, spine or other nerves, neuro-sensors that perform electroencephalogram (EEG) measurements, and drug infusion pumps that deliver precise doses of drugs at consistent time intervals. Despite dramatic technological advances in all of these device types through the years, most of the devices are still relatively large, with volumes ranging from about 15cc to 50cc [1,2] – roughly the volume of two AA batteries to the volume of two C batteries. These large devices still typically require invasive surgical implant procedures, and have inherent reliability challenges related to their long leads or catheters.

MIMDs

The new generation of MIMDs can be implanted at the point of therapy or sensing, thus eliminating the need for long leads, and enabling minimally invasive surgical procedures. Examples of such devices include; an EEG monitor with tiny leads implanted above the scalp, a drug infusion pump with a tiny catheter implanted in the eye socket, and a neuro-stimulator implanted in the neck. To enable remote placement, the new MIMDs usually require device volumes less than 4cc – roughly the volume of one AAA Battery.

Enabling Technologies

The latest MEMS, packaging, and battery technologies are the primary enablers for most of the MIMD miniaturization. MEMS sensors, such as accelerometers, pressure sensors, and fluid flow sensors are very small electrical and mechanical built to scales comparable to ICs, and thus can be significantly smaller than traditional sensors performing the same functions. Chip scale package (CSP) technology enables IC Packages that are virtually the same size as the ICs contained within them [3], and stacked chip scale package (SCSP) technology enables the placement of multiple ICs in a single package [4]. Finally, new solid-state chip-scale batteries are now available in sizes about 10 times smaller than traditional IMD batteries [5]

Custom Electronics

To maximize the benefits of these new technologies, the electronic circuits in MIMDs must be designed specifically to their unique characteristics and requirements. For example, a MEMS flow sensor is likely to require a specific supply voltage and current range, provide a specific range of output voltages, and require specific signal filtering and processing. Customized circuits contained in Application Specific Integrated Circuits (ASICs) are often required to interact with such devices without wasting power and/or size. For the most size-efficient SCSPs, the bond pads of the various ICs must be placed to optimize all of the connections between internal ICs as well as between each IC and the package pins. Most importantly, while solid-state batteries offer significant size reduction, the capacity of these batteries is extremely limited. Typical neuro-stimulators include batteries with capacities ranging from about 40mA-H to 220mA-H [6], but solid-state battery capacities are typically less than 0.05mA-H [7]. Solid-state battery technology can be combined with SCSP technology to produce battery stacks which can provide an incremental capacity increase at the cost of an incremental size increase. However, the battery stack approach is practically limited to about 20 batteries per MIMD, for a maximum battery capacity of about 1mA-H.

Power Reduction

Power reduction is one of the major challenges for any IMD because the power consumption of the implanted devices is directly related to the size of the battery required, and the battery can be the largest component in the device [8]. Higher device power consumption requires higher battery capacity, and higher battery capacity requires larger battery volume. So, generally speaking, size reduction requires power reduction. For MIMDs with a goal of using solid-state batteries, power reduction becomes the primary circuit design problem.

Design Opportunities

The extreme size reduction required by MIMDs presents many design challenges. One of the keys to a successful design is to identify opportunities and use them to our advantage. These opportunities arise from specific conditions and characteristics

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unique to many MIMD applications. For example, while most industrial ICs require an operating range from -40C to 85C, the critical operating temperature of implantable devices is usually limited to a small range around body temperature (37C). Since most semiconductor device parameters vary with temperature, the limited operating temperature range of MIMDs alleviates a significant design challenge.

MIMDs usually interface to slow biological systems in the body, so signal frequencies required for sensors and drivers are typically less than 200Hz. The low frequency measurements and therapies can often be supported by system clocks of 100KHz or less, while many industrial applications require system clocks of 10MHz or more.

The biological systems in the body typically do not require extreme precision either. For example, many cardiac pacemakers and neuro-stimulators can tolerate stimulus errors of 0.5% or more, so the stimuli can be derived from digital to analog converters (DACs) with only 8 bits of precision. The precision required for ECG and EEG is usually higher, but it is still common for these measurement systems to use analog to digital converters (ADCs) with only 12 bits of precision. In contrast, audio systems routinely require 16-bit DACs and 24-bit ADCs.

In addition to the moderate performance requirements of MIMDs, there are some details about the use of MIMDs that we can take advantage of. Many MIMD systems include micro-controller units (MCUs) that contain some non-volatile memory (NVM). The NVM allows the device memory to be maintained even when power is removed from the MCU, so the system can be designed such that the MCU can be disabled at all times except when it's function is absolutely necessary. The ASIC design can also employ the NVM to hold calibration data for analog measurement and stimulation circuits. The MIMD can thus be calibrated prior to implant, and the calibration will be maintained for the life of the device. Since the MIMDs are typically calibrated in this manner, the analog circuit performance can be degraded, as long as the calibration has the range and resolution necessary to meet the final post-calibration accuracy requirements. The reduced analog accuracy requirements can enable significant size and power reductions in the analog circuits.

Finally, most MIMDs contain rechargeable batteries, and these batteries require periodic recharging – commonly once per day. The recharging process requires wireless energy transfer from an external electronic module typically referred to as a charger. Since the charger must be linked to the MIMD frequently, we can superimpose wireless communication on the wireless charger link, and use that communication link to periodically re-calibrate analog circuits as needed. The accumulation of timing or measurement errors can thus be limited to a 24-hour period, rather than for the multiple-year life of the device.

Presented here are some circuit design approaches that help to capitalize on the available opportunities, and enable the dramatic miniaturization required for the new generation of MIMDs.

Output Driver

Figure 1 is a block diagram of a typical output driver circuit for a neuro-stimulator device. The function of the output driver is to sink or source a programmable constant current through a resistive load presented by neurological tissue in the body. In this example, the current sink and source amplitude can be set up to 3mA, and the typical load is about 1.5K ohms. This configuration requires two positive supplies, VREF and VSTIM. The voltage between VREF and GND must be at least large enough to support the voltage required at the load plus the overhead voltage required to operate the current sink – in this case, $3\text{m} \times 1.5\text{K} + 1\text{V} = 5.5\text{V}$. The same voltage is required between VSTIM and VREF, so the whole circuit needs an 11V and a 5.5V supply. Since MIMD battery voltages typically operate in the range of 3.6V to 4.2V, the device must include two boost converters to multiply the 3.6V minimum battery voltage up to 11V and 5.5V. A similar analysis applies to output drivers for higher-current neuro-stimulators.

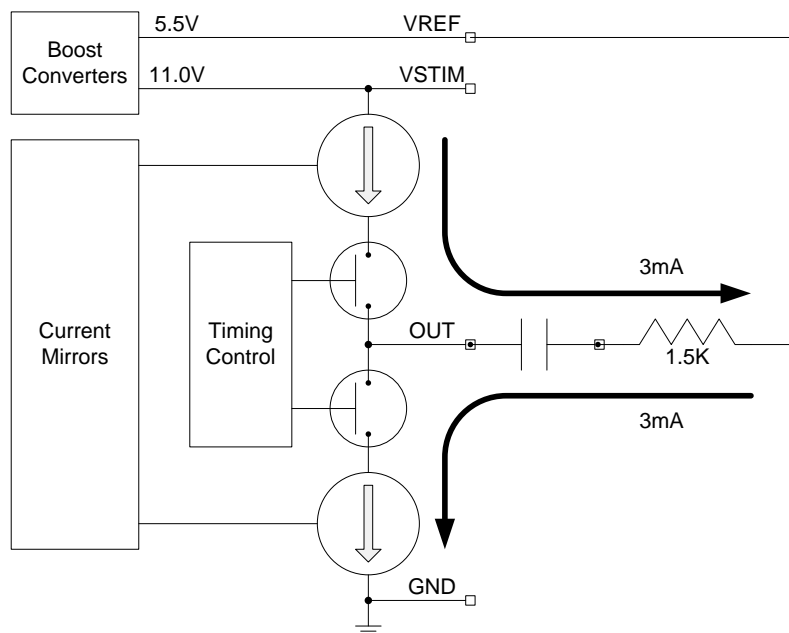


Figure 1: Output Driver

Figure 2 shows an alternate Output Driver design, typically referred to as an h-bridge. The h-bridge performs the same function as the typical output driver, but only requires one supply, VSTIM. In this case, the voltage between VSTIM and GND only needs to be $3\text{m} \times 1.5\text{K} + 1\text{V} + 1\text{V} = 6.5\text{V}$ and the device only requires one boost converter.

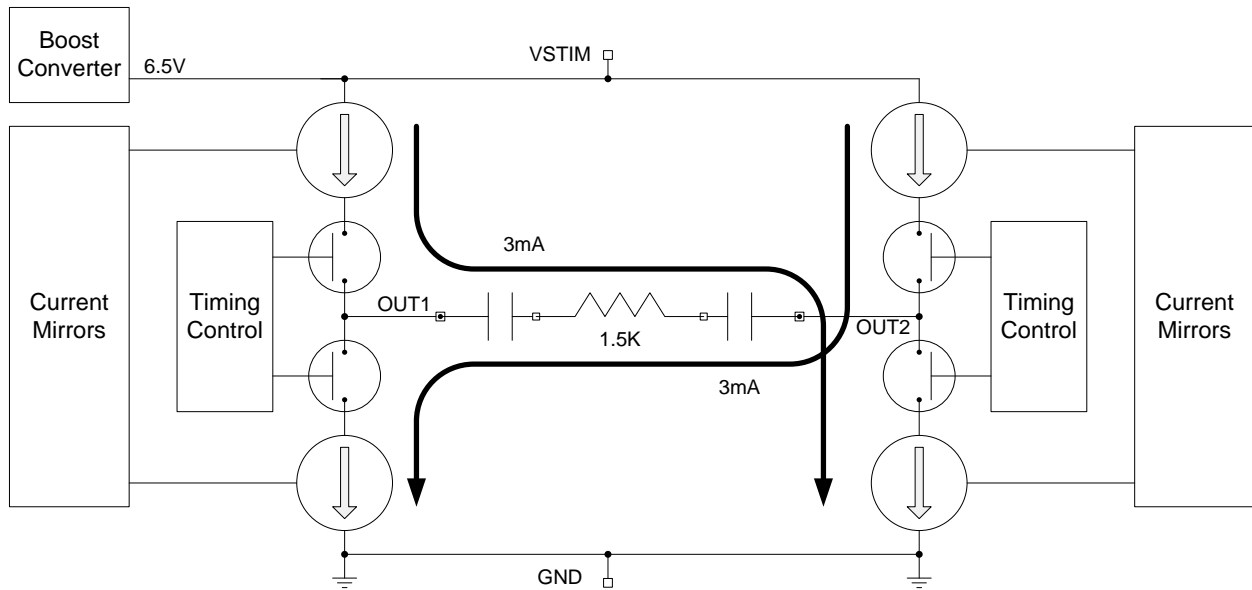


Figure 2: H-Bridge Output Driver

Current DAC

Figure 3 is a block diagram of a typical current DAC (IDAC) circuit for a neuro-stimulator device. The function of the IDAC is to convert a binary digital value into a proportional analog current to provide the input voltage for the output driver circuit. In this example, the IDAC is supplied by the same VSTIM supply as the output driver, and the IDAC output multiplier is limited to 10x to maintain good matching performance. The precision of the IDAC is proportional to the matching of the binary-weighted devices, N_0 through N_7 . The matching performance of MOS devices is inversely proportional to the square root of the gate area of the unit device [9], so the unit device must be large enough to provide at least 8-bit precision. Because the IDAC is supplied by VSTIM, which is typically greater than 3.3V, the circuit cannot use low-voltage devices. Instead, the circuit must use medium-voltage or high-voltage devices which, due to their structure, do not match as well as low-voltage devices, and also have a larger overall footprint for the same gate areas as low-voltage devices. A circuit area estimate for the IDAC in this example is 0.250 square-microns. The overhead power for this approach is roughly 10%, or about 2mW to drive 20mW to the output load.

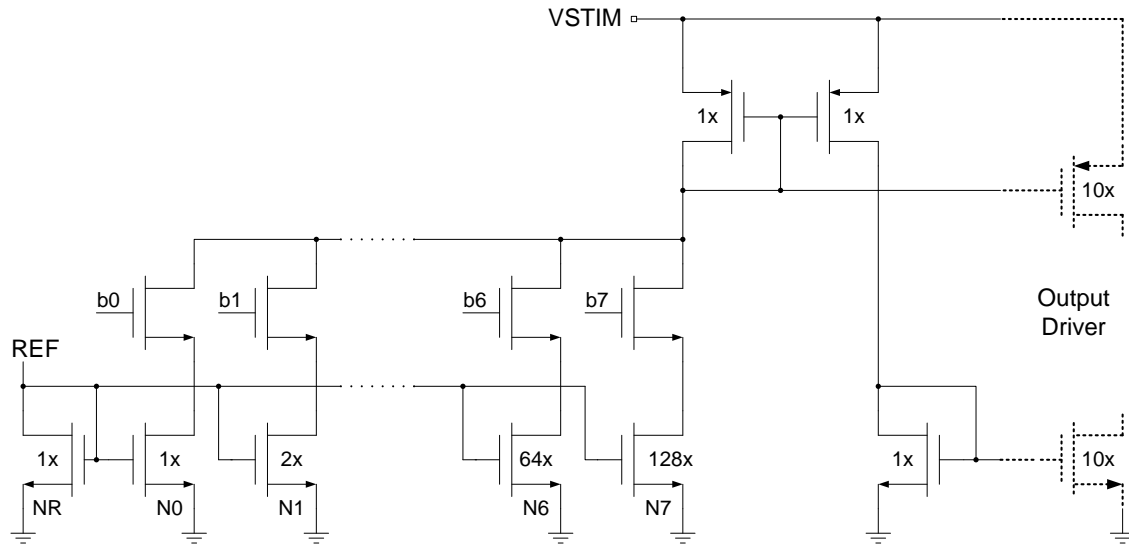


Figure 3: High Voltage Current DAC

Figure 4 shows an alternate approach for the IDAC. Because most applications never require the source and sink currents for a single output to be on simultaneously, the circuit can be reduced to include only one IDAC that can be programmed to alternate between the source and sink amplitudes. With the addition of a level-shifting current multiplier circuit, the IDAC can be changed to run on a low-voltage supply. The low-voltage supply enables the use of low-voltage devices that match better than medium-voltage devices, and are smaller overall for the same gate area. A circuit area estimate for the IDAC in this example is only 0.025 square-microns, about 10 times smaller than the Figure 3 example. The current level-shifter approach also supports a higher current multiplier. In this case, the circuit includes a 40x current multiplier, so the overhead power is reduced to roughly 2.5% or only 0.5mW to drive 20mW to the output load.

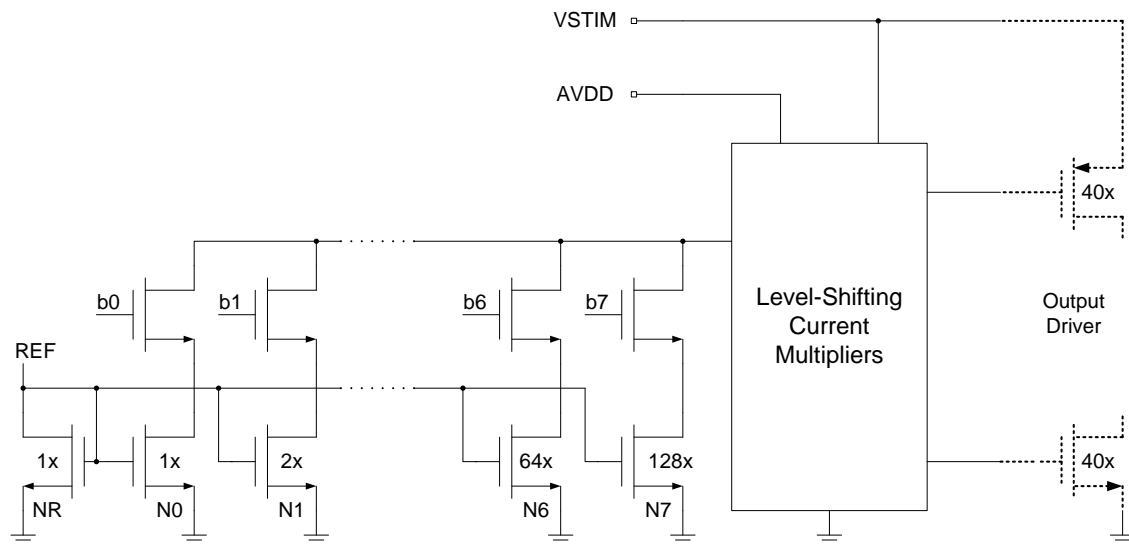


Figure 4: Low Voltage Current DAC

Oscillator

Figure 5 is a block diagram of a typical crystal oscillator circuit for an IMD. This approach is very common in IMDs because the crystal oscillator provides extremely high frequency accuracy. High frequency accuracy is usually required because IMDs are often required to keep track of the real time to match up with therapy delivery and/or sensor measurement information. If the oscillator frequency has a small error, the error accumulates over the life of the device. For example, a 0.1% oscillator frequency error causes the time of the device to mismatch real time by almost 9 hours per year. With a crystal oscillator, frequency errors are typically less than 0.005%, so annual time mismatch is less than 30 minutes. The crystal oscillator circuit requires a 32KHz crystal in addition to the integrated amplifier circuitry. It also requires two IC pins to make the connections between the crystal and the circuit. The crystal oscillator is typically required to be enabled 100% of the time, and commonly consumes about 1uW of battery power.

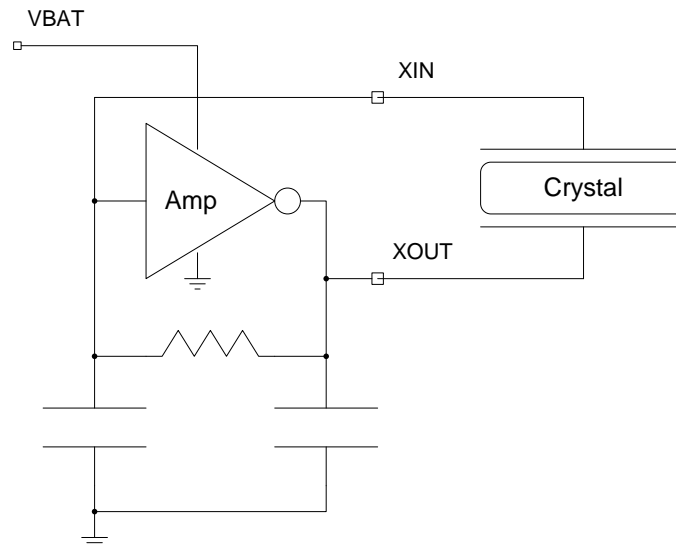


Figure 5: Crystal Oscillator

Figure 6 is a block diagram of an alternative to the crystal oscillator. This ultra-low-power (ULP) oscillator takes advantage of the periodic recharge required by most IMDs. Since the periodic recharge can also be used to re-calibrate the device time to agree with a more accurate timing reference in the charger, the oscillator's frequency accuracy requirement can be relaxed substantially. For example, a one minute per day accuracy requirement can tolerate an oscillator frequency error of 0.07%. With the relaxed accuracy requirements, the oscillator design no longer requires a crystal, and can be designed to consume only about 200nW of battery power. Compared to a crystal oscillator, this ULP oscillator eliminates the crystal, and one ASIC pin, and reduces the battery power by 80% in timekeeping mode.

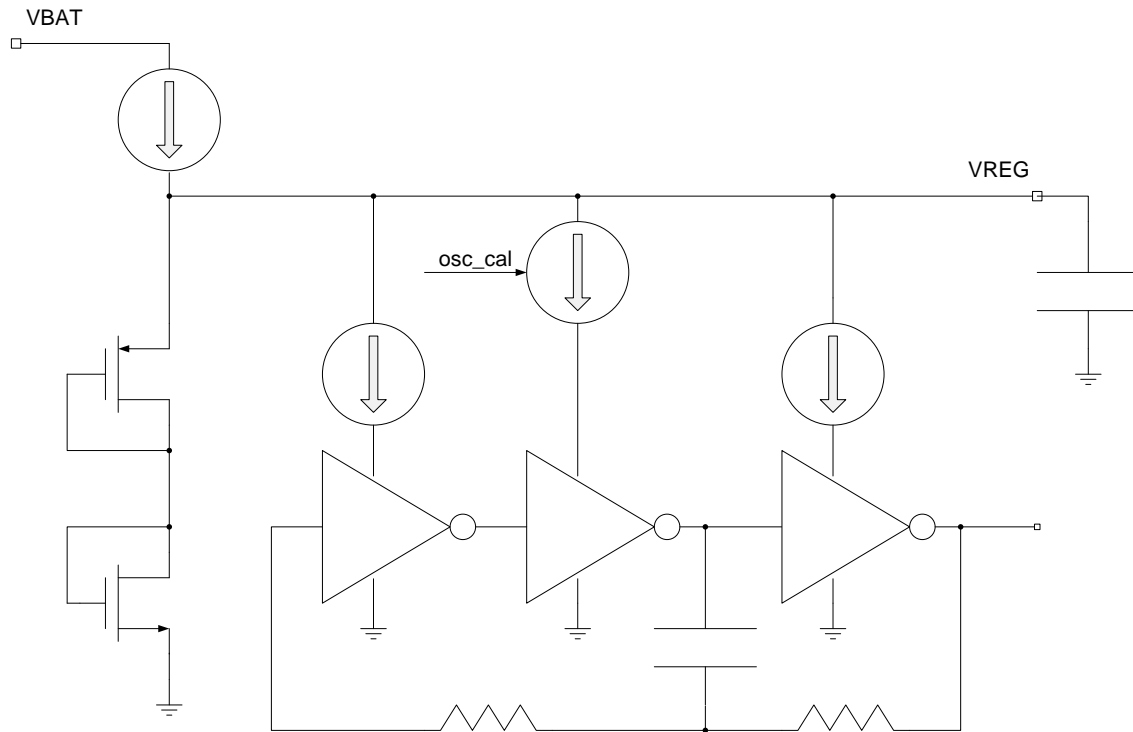


Figure 6: Ultra-Low-Power Oscillator

Communication

Most IMD systems support two-way wireless communication between the implanted device and the charger or programmer. Many of the IMDs feature radio frequency (RF) communication in the Medical Device Radiocommunications Service (MedRadio) frequency spectrum, which ranges between 401MHz and 457MHz. The MedRadio spectrum was established by the Federal Communications Commission (FCC) for diagnostic and therapeutic purposes in IMDs [10]. Figure 7 is a circuit board layout diagram of a typical IMD including a radio frequency integrated circuit (RFIC) to support 2-way communication between the IMD and an external charger or programmer. This type of device supports high data rates – up to about 500Kbps, and long distance communication – up to about 2 meters [11], but the device minimization is limited by the relatively large battery and number of components. This example includes a 4mm x 4mm ASIC, a 4mm x 4mm MCU, a 4mm x 4mm RFIC, and a 1cc/40mW-H battery. The system also requires two crystals and two antennas to support the timekeeping, recharging, and communication functions. The overall volume of this example would be approximately 3.2cc. The typical battery power consumed during communication for this type of device is about 40mW [11]. Recently, some RFICs with built-in MCUs have been released. These products combine the features of the RFIC and the MCU in a single IC measuring about 6mm x 6mm. While this approach can help reduce the circuit dimensions, the power required for high-rate, long-distance communication still typically eliminates the possibility of using solid-state batteries.

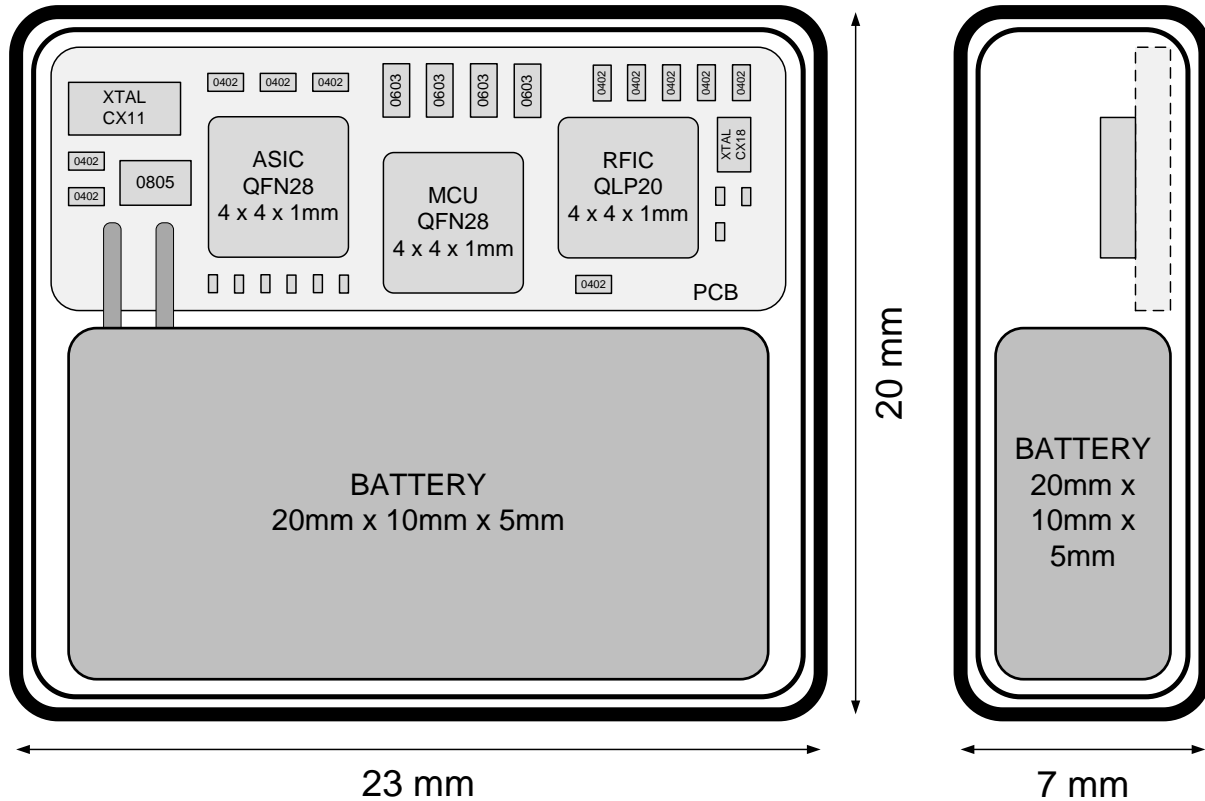


Figure 7: IMD with RFIC Link

For systems that can tolerate a lower data rate – less than about 10Kbps, and a shorter communication distance – less than about 10cm, an MIMD can be designed with a near-field magnetic induction (NFMI) link. The NFMI link uses magnetic induction between a coil in the MIMD and a coil in the charger. This type of link was popular in early IMD products, but is now less prevalent in mainstream IMD products, due to the availability of suitable RFIC technology, and the desire for high data rates and long distance communication links. Despite the technology’s old roots, the NFMI link is an excellent enabler of IMD miniaturization. Figure 8 is a circuit board layout diagram of an MIMD that uses an NFMI link. Relative to the Figure 7 example, this approach replaces the RFIC with a small amount of circuitry that is readily integrated into the ASIC. This solution takes advantage of the fact that communication is only required when the charger is present. The communication link shares the antenna with the charging function and requires no internal clock, so it eliminates the need for one crystal, and one antenna. The NFMI uses a passive load-shift-key (LSK) protocol, which only uses power from the charger, so no battery power is required for communication [12]. This example includes three 0.06cc/50uA-H solid-state batteries, with significantly lower capacity enabled by replacing the RFIC with an NFMI link. The overall volume of this example would be approximately 1.8cc.

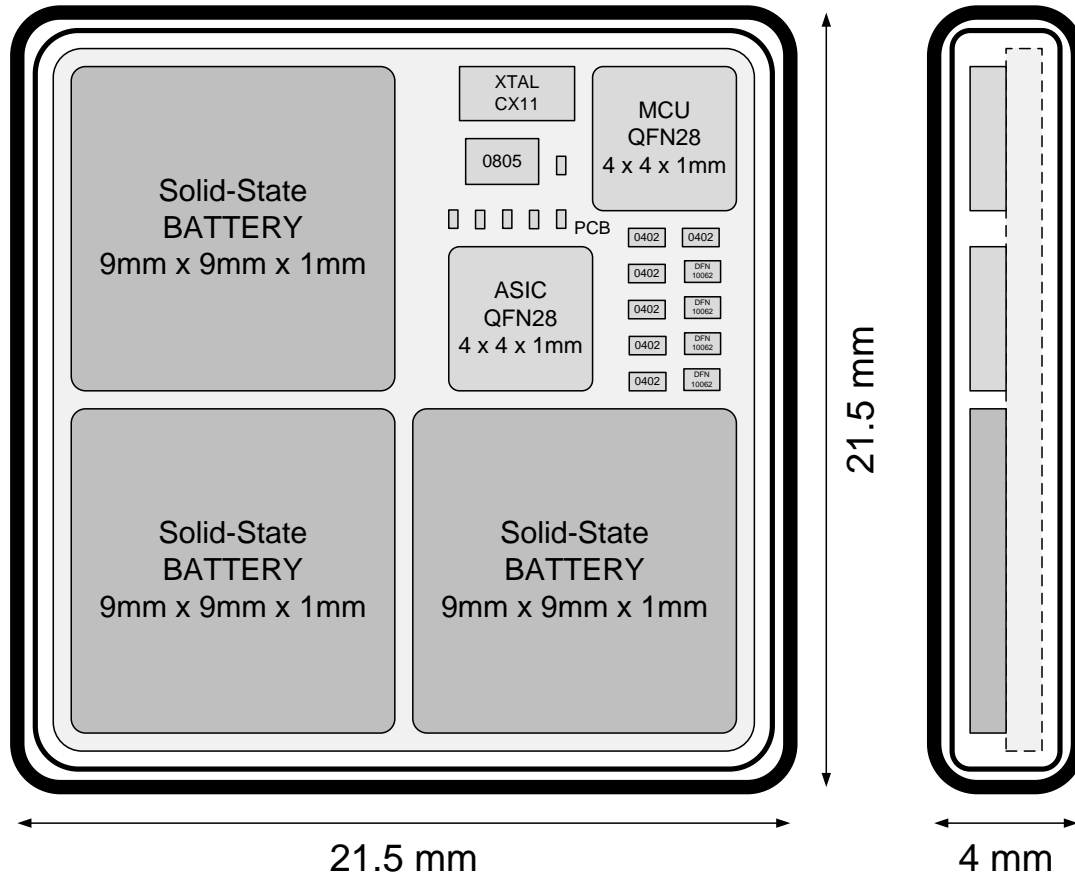


Figure 8: MIMD with NFMI Link

Power Management

In addition to these power-saving circuits, MIMDs generally require a thorough system-level power management approach. To fully optimize the size and power of the MIMD, the power management usually requires customization that takes into account the specific requirements, challenges, and opportunities of each unique system. For example, neuro-stimulator output drivers typically require supplies that are greater than the battery voltage, but the MCU interfaces typically require supplies that are lower than the battery voltage. It is therefore common for an ASIC in an MIMD to contain both voltage boost and voltage buck circuits. These voltage conversions can be done with a variety of circuits, including inductive boost or buck converters, capacitive boost or buck converters, and linear voltage regulators. All of these circuits have strengths and weaknesses, and the appropriate selection and combination of the circuits is critical to achieve the power reduction required for most MIMDs. In addition to the voltage conversions, the power management should include very careful control of the power sequencing such that each sub-circuit is enabled only when it is absolutely necessary, and is disabled at all other times.

MIMD Example

Figures 9 and 10 are a block diagram and circuit board layout of an MIMD that employs some of the techniques described in this paper. The device is a neuro-stimulator with a device volume of less than 1cc, making it small enough to be implanted at the point of therapy. The device includes an MCU in a wafer-level-chip-scale-package (WLCSP) [13], an ASIC in a custom MicroLeadFrame® (MLF) package [14], and a die-stack of solid-state batteries. The MIMD features neuro-stimulation with 8-bit programmable amplitudes up to 3mA at 6.5V. The device is rechargeable with an external charger, and lasts up to 3 days between recharge sessions for a typical stimulation therapy of 1mA at 1% pulse duty cycle and 100% therapy duty cycle.

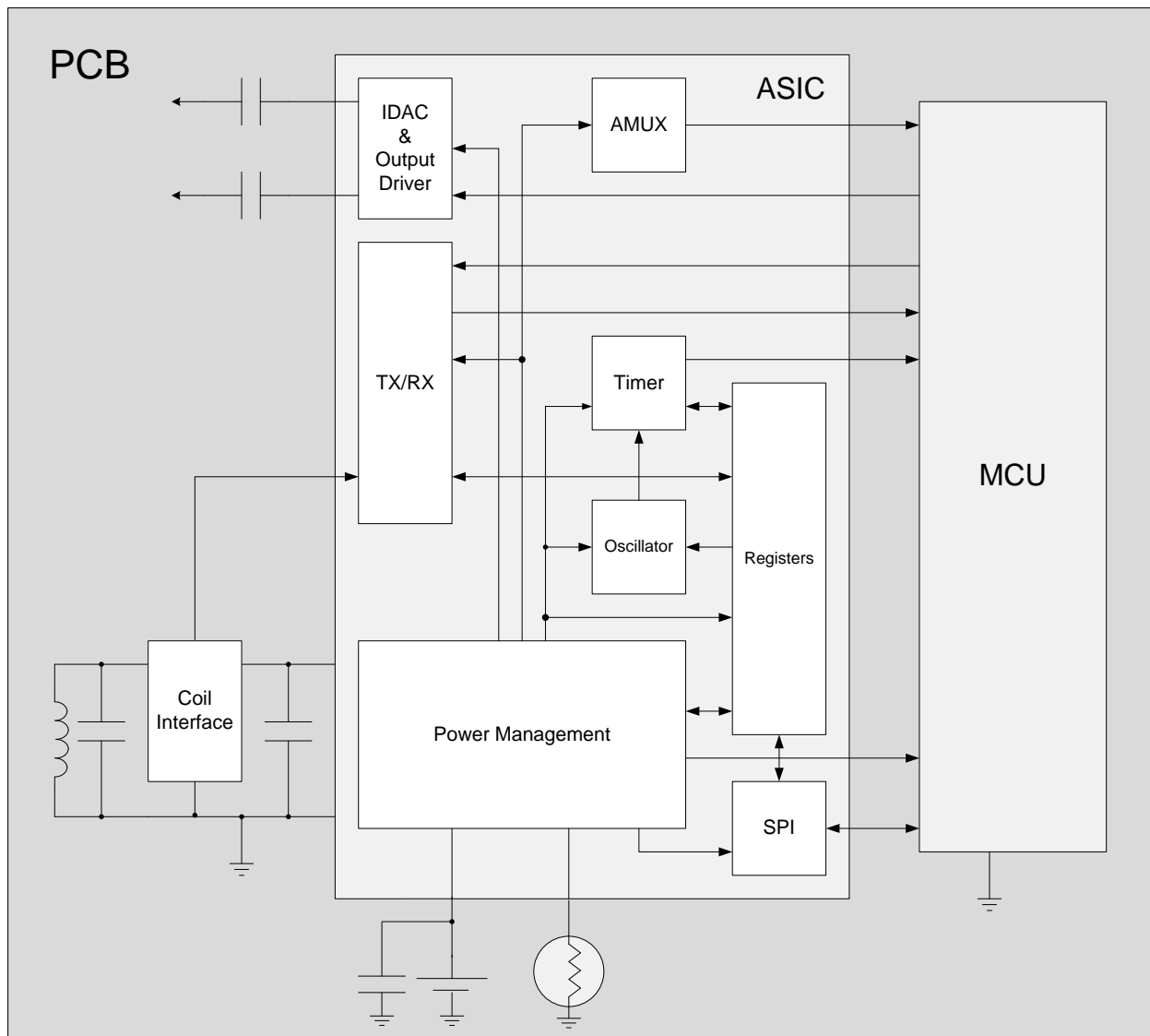


Figure 9: MIMD Block Diagram

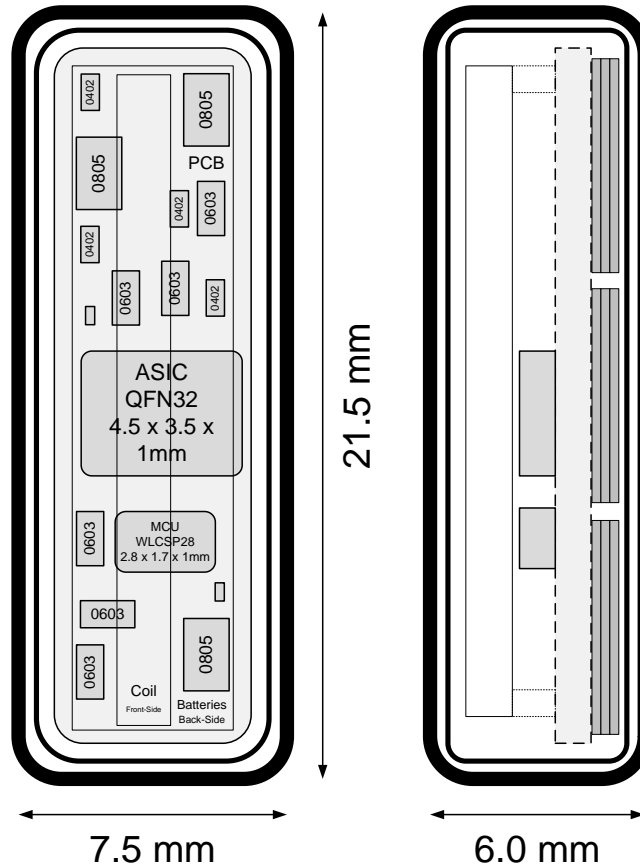


Figure 10: Neuro-Stimulator MIMD

Conclusions

The dramatic miniaturization required to make practical MIMDs presents a wide range of design challenges, but new technologies are available to enable that miniaturization. The most effective use of the new technologies typically requires a level of integration and customization only achievable with ASIC design. The requirements of MIMDs vary greatly depending on the application, and there is no single approach or solution that will work for all cases. However, this paper presents several circuit ideas that help capitalize on new technologies and application-specific design opportunities, and demonstrates a practical solution for a small MIMD with a volume of less than 1cc.

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