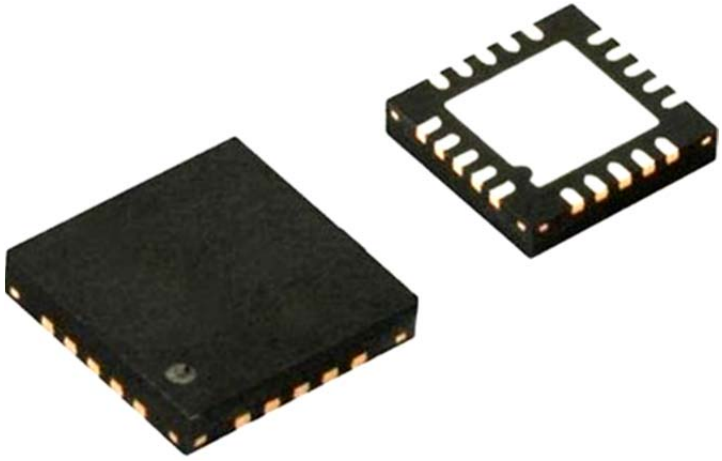
CSI021

4-Channel High Voltage Programmable Current Sink/Source

CSI021 NeuroStim ASSP Datasheet Rev 1.3

FEATURES

- 4 Output Channels per IC
- Independent 8 Bit DAC Programmability
- SPI Programmable Output Current Range
- High Output Current [up to 6mA]
- High Output Voltage [up to 18V]
- Programmable Pulse Widths
- Programmable Pulse Frequencies
- Programmable On/Off Periods
- Programmable Amplitude Ramp-Up
- Integrated Charge Balancing
- Low Voltage SPI Interface [2.5V]
- Low Overhead Power [< 10mW]
- Ultra-Low Standby Power [< 25µW]
- Real time status bits for all four channels
- SPI Writable Trigger Register to synchronize channels & multiple ICs



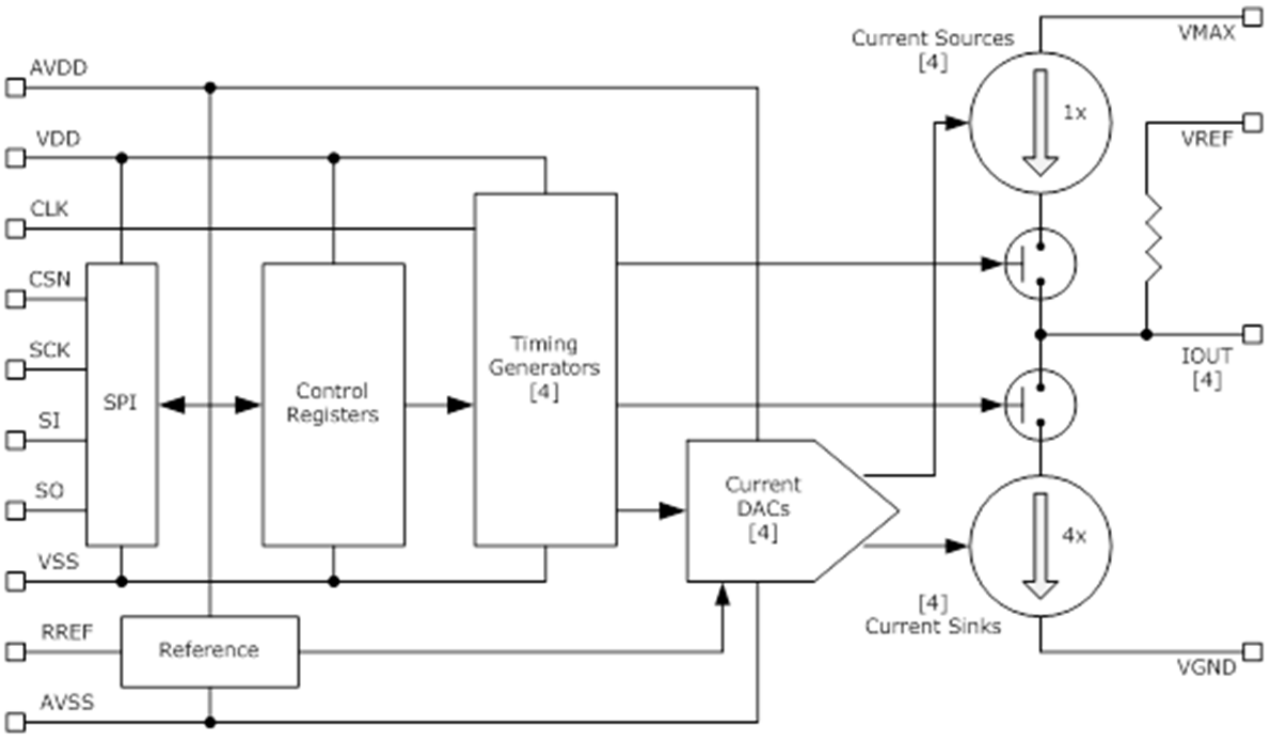
APPLICATIONS

- Neurostimulation/Neuromodulation
- Implantable Pulse Generator/IPG
- MEMS and Sensor Applications
- Battery Powered Applications

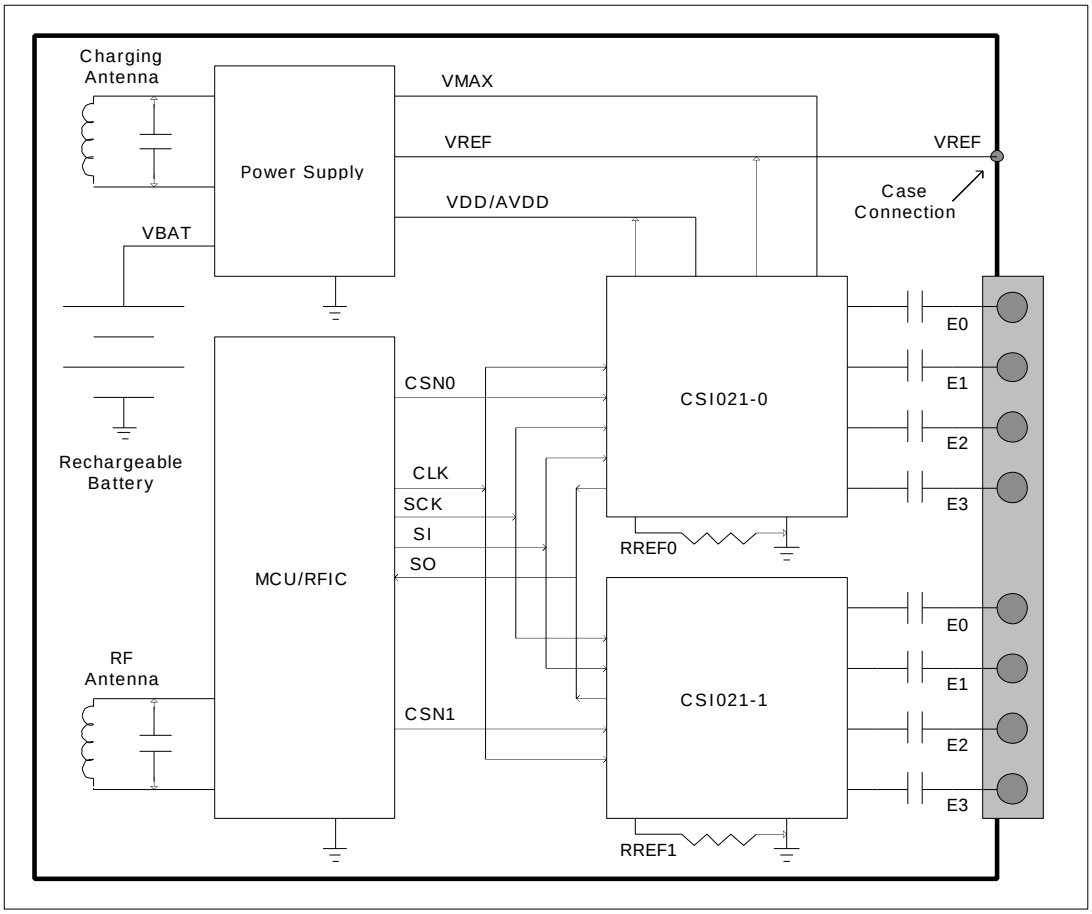
GENERAL DESCRIPTION

The CSI021 features 4 independent 8-bit linear DAC programmable current sink/source outputs with up to 6mA full-scale sink, and 1.5mA full-scale source currents. Full-scale current ranges are also adjustable via an external reference resistor. An 18V supply voltage allows for 6mA output currents into 1.5kΩ loads. The CSI021 pulse timing is fully programmable via a 10MHz, 2.5V SPI, such that all timing parameters are proportional to the input clock period. Programmable parameters include sink/source pulse widths, pulse frequencies, stimulation on/off periods, and amplitude ramp rates. Internal timing generators in the CSI021 use the programmed parameters to create therapy profiles with only minimal intervention from a host processor, and a 4:1 sink to source current ratio provides for easy stimulation charge balancing.

FUNCTIONAL DIAGRAM



TYPICAL APPLICATION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

DESCRIPTION	MIN	MAX	UNIT	NOTE
Digital Inputs	-0.5	5	V	Relative to GND
Electrode Outputs	-0.5	20	V	Relative to GND
VMAX, VREF Supplies	-0.5	20	V	Relative to GND
VDD, AVDD Supplies	-0.5	5	V	Relative to GND
RREF Pin	-0.5	5	V	Relative to GND
Storage Temperature	-25	125	^{o}C	

COMPONENT REQUIREMENTS

COMPONENT (Typical)	VALUE	UNIT	RATING	TYPE
Electrode Output Capacitors [4]	1	µF	25V	X5R
Reference Resistor	2.0	MΩ	1/8 W	1%

PIN DESCRIPTIONS

PIN #	NAME	DESCRIPTION	PIN #	NAME	DESCRIPTION
1	CSN	SPI Chip Select (Not) Input	11	IOUT3	Current Sink/Source Output3
2	SCK	SPI Clock Input	12	IOUT2	Current Sink/Source Output2
3	SI	SPI Slave Input	13	IOUT1	Current Sink/Source Output1
4	SO	SPI Slave Output	14	IOUT0	Current Sink/Source Output0
5	CLK	Clock Input	15	VREF	Current Source Reference [12V]
6	VGND	Circuit Ground	16	VMAX	Current Source Supply [18V]
7	VGND	Circuit Ground	17	NC	No Connect
8	RREF	Ref. Resistor Connection	18	NC	No Connect
9	AVDD	Analog Supply [2.5V]	19	NRST	Digital logic NRST pin
10	VGND	Circuit Ground	20	VDD	Digital Supply [2.5V]

OPERATING CONDITIONS

DESCRIPTION	MIN	TYP	MAX	UNIT	NOTE
VDD/AVDD Voltage	2.4	2.5	2.6	V	Regulated supply
VMAX	17	18	19	V	
VREF	11.9	12.6	13.3	V	
Logic 0 Input Voltage	0		0.4	V	
Logic 1 Input Voltage	VDD-0.4		VDD	V	
Fclk (CLK Frequency)	10	100	400	kHz	
Tclk (CLK Period)	2.5	10	100	µs	Stimulation timing proportional to CLK period
RREF Resistance		2		MΩ	
Output Load Resistance	1		1.5/3	kΩ	1uF cap to VREF, For Boost mode the load is limited to 1.5kΩ.
Operating Temperature	10		50	^{o}C	
Power-Up Delay	25			µs	VDD/AVDD to VMAX/VREF

VMAX & VREF LIMITATIONS

The valid operating range for VMAX and VREF is constrained by the maximum anticipated sink/source output current and the load resistance into which this current flows. The following equations set the boundaries on VREF and VMAX, where V_{DO} corresponds to the drop-out voltage of the output devices, and ISNK and ISRC correspond to the sink and source stimulation currents respectively.

$$\boldsymbol{VREF_{MIN} = V_{DO} + (ISNK_{MAX} * R_{LOAD})} \quad \text{..... (1)}$$

$$\boldsymbol{VMAX_{MIN} = VREF + V_{DO} + (ISRC_{MAX} * R_{LOAD})} \quad \text{..... (2)}$$

As shown in the electrical specifications table, the output current variation can be reduced by lowering VREF if the maximum load current or maximum load resistance is properly restricted. Under these same conditions, and with VREF reduced, VMAX can also be lowered to save power.

ELECTRICAL SPECIFICATIONS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VDD Off-state Current	CLOCK and SPI disabled			10	nA
AVDD Off-state Current	PDN = 0			200	nA
VMAX Off-state Current	All Channels disabled			10	nA
VDD Dynamic Current	Fclk= 100kHz, All Channels Enabled			50	µA
AVDD Current	PDN = 1, All Channels Enabled			100	µA
VMAX Current1	Full scale AMP, Excludes IOUT			350	µA
VMAX Current2	Full scale AMP, Excludes IOUT			500	µA
Current Sink Resolution			8		bits
Current Sink Range	Full scale AMP, BOOST_EN=0		3.06		mA
Current Sink Range	Full scale AMP, BOOST_EN=1		6.12		mA
Current Sink Step Size	BOOST_EN=0		12		µA
Current Sink Step Size	BOOST_EN=1		24		µA
Current Sink Matching Error	Channel to channel, same conditions			10	%
Current Sink Non-Linearity Error	IOUT = -3.06mA, VMAX=18V, VREF=2.5V to 15.5V, RL=0Ω	-5		5	%
Current Sink Non-Linearity Error	IOUT = -6.12mA, VMAX=18V, VREF=2.5V to 15.5V, RL=0Ω	-10		10	%
Current Sink Dropout Voltage	IOUT = -3.06mA, RL=0Ω			2.5	V
Current Sink Regulation Error1	AVDD Supply 2.4V – 2.6V			0.5	%
Current Sink Regulation Error2	VMAX Supply 17V – 19V			2.5	%
Current Sink Temp Regulation Error	T = 10C - 50C			1	%
Current Sink Output Leakage	Output Switch off			20	nA
Current Source Resolution			8		bits
Current Source Range	Full scale AMP, BOOST_EN=0		0.77		mA
Current Source Range	Full scale AMP, BOOST_EN=1		1.54		mA
Current Source Step Size	BOOST_EN=0		3		µA
Current Source Step Size	BOOST_EN=1		6		µA

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Current Source Matching Error	Channel to channel, same conditions			10	%
Current Source Non-Linearity Error	IOUT = 0.77mA, VMAX=18V, VREF=2.5V to 15.5V, RL=0Ω	-5		5	%
Current Source Non-Linearity Error	IOUT = 1.54mA, VMAX=18V, VREF=2.5V to 15.5V, RL=0Ω	-10		10	%
Current Source Dropout Voltage	IOUT = 0.77mA, RL=0Ω (V_{DO} = VMAX–VOUT)			2.5	V
Current Source Regulation Error1	AVDD Supply 2.4V – 2.6V			0.5	%
Current Source Regulation Error2	VMAX Supply 17V – 19V			2.5	%
Current Source Temp Regulation Error	T = 10C - 50C			1	%
Current Source Output Leakage	Output Switch off			20	nA
Sink Current Settling Time	IOUT=-3.06mA			2	µs
Source Current Settling Time	IOUT=0.77mA			2	µs
Output Discharge Resistance	To VREF, Output Switches off	0.5	1.0	1.5	MΩ
Digital Input Pull-Down Resistance	All digital Inputs	2	4	6	MΩ

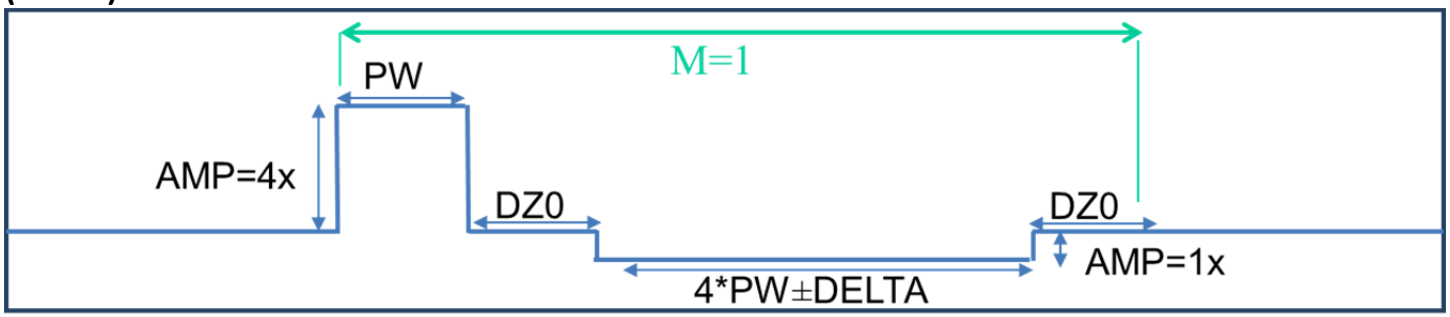
TIMING SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNIT
SPI_CLK Frequency		1.0	10	MHz
Input Setup Time		250		nS
Input Hold Time		250		nS
Output Valid Time		100		nS
Output Hold Time		0		nS
Output Rise/Fall Time		100		nS

STIMULATOR PULSE TIMING

For each channel, the Stimulation Amplitude, Pulse Width and Dead Zone are programmable via SPI. The recharge width is automatically set to 4*PW. The parameter DELTA if set, allows for +/-25% change in the recharge width.

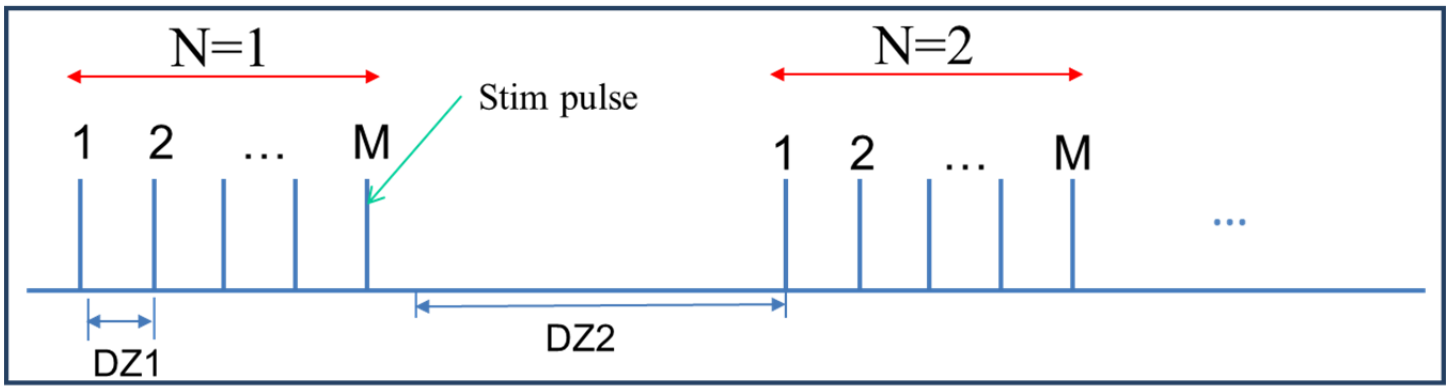
Parameters: Amplitude (AMP), Pulse Width (PW), Dead Zone (DZ0), Recharge Width adjustment (DELTA)



STIMULATOR THERAPY TIMING

In the therapy timing diagram, M represents number of consecutive stimulation pulses separated by a delay of DZ1. N is the number successive sets of M pulses each, separated by a delay of DZ2. The parameters DZ1 and DZ2 can be set via SPI for each channel.

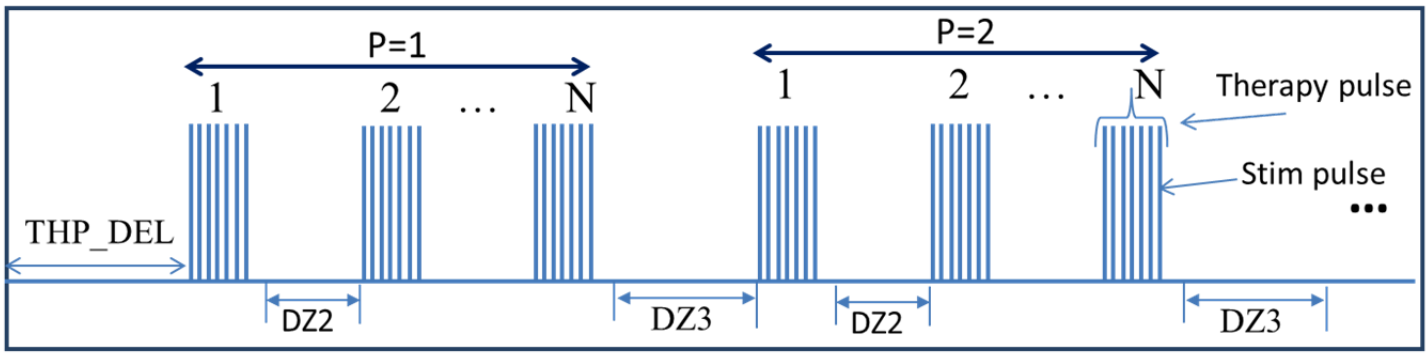
Parameters: Dead Zone 1 (DZ1), Number of sink/source periods (M), Dead Zone 2 (DZ2), Number of consecutive periods (N)



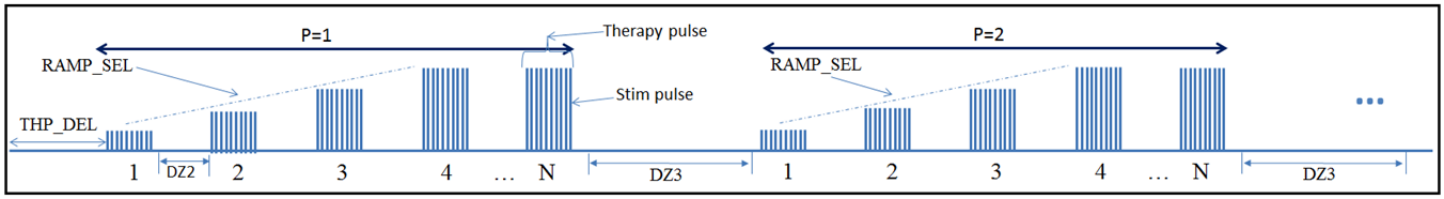
STIMULATOR MASTER TIMING

For the master timing diagram, P is the number of master pulses each containing N sets of M pulses each. DZ3 can be programmed via SPI for each channel to adjust the delay between the master pulses. When the specified number of master pulses is finished, the therapy is completed. There is a mode in which the stimulation amplitude can be ramped up to the final value specified by the AMP parameter. The RMP_SEL register lets you select the ramp mode individually for each channel. When RMP_SEL is set, first four sets in each master pulse are ramped from 0.25*AMP to AMP in steps of 0.25*AMP. The division is achieved by shifting bits of the amplitude register and therefore is not exact. In case N<4, the amplitude will not reach its final value.

Parameters: Therapy Delay (THP_DEL), Dead Zone 3 (DZ3), Ramp Select (RMP_SEL), Number of Master pulse periods (P)

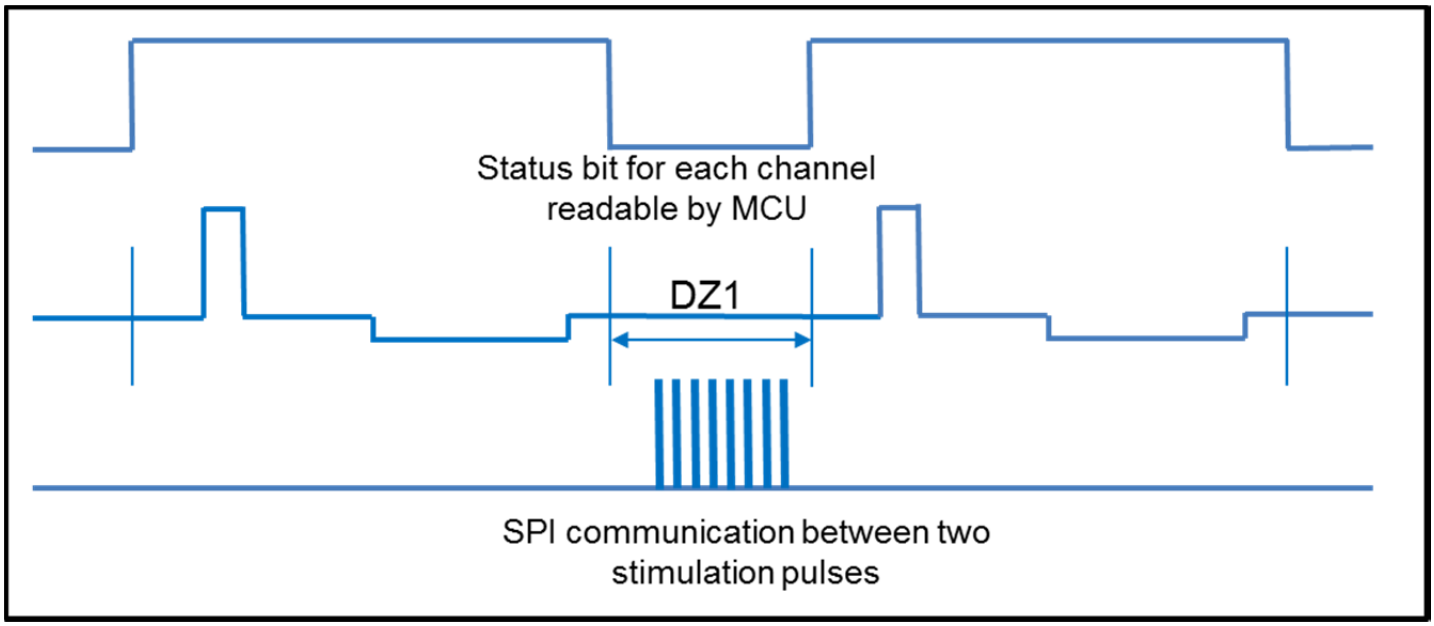


Pulse waveform when RMP_SEL is set:



STATUS BITS

A real time status bit is available for each channel as a read only register (8'h3E, ASIC_STAT). This register can be read by the microprocessor to detect end of stimulation and use SPI to reprogram the parameters to generate custom stimulation pattern. This is feasible only when the DZ1 parameter is set to be greater than 2 times the step size for DZ1. This is because the status bit stays high if DZ1 is set to anything lower than 2 indicating continuous stimulation. The SPI communication can operate at speeds up to 10MHz which gives enough time to update required parameters.



ASSP PROGRAMMABLE PARAMETERS

The following table specifies the range and step sizes for each of the programmable parameters. These parameters can be individually set for every channel.

NAME	DESCRIPTION	STEPS	DEFAULT	STEP SIZE	RANGE
AMP	Sink Pulse Amplitude	255	0	12µA	0 to 3.06mA
		255	0	24µA	0 to 6.12mA
PW	Sink Pulse Width	255	1	Tclk	0 to 255*Tclk
DZ0	Dead zone between sink and source pulses	255	0	Tclk	Tclk to 255*Tclk
DELTA	Recharge Width Adjustment, Positive or Negative	127	0	Tclk	0 to 127*Tclk
DZ1	Dead zone between sink/source periods (PPER)	255	0	8*Tclk	Tclk to 2,040*Tclk
M	Number of consecutive sink/source periods	255	1	1	1 to 255
DZ2	Dead zone between sets of sink/source periods	255	0	4,096*Tclk	Tclk to 1,044,480*Tclk
THP_DEL	Delay from start of therapy to first stimulus delivered	255	0	4,096*Tclk	10*Tclk to 1,044,480*Tclk
N	Number of consecutive periods	255	1	1	1 to 255
DZ3	Dead zone between therapy pulse sets	255	0	2,097,152*Tclk	0 to 534,773,760*Tclk

Note: Tclk = Period of CLK input = 1/Fclk

REGISTER DEFINITIONS

#	ADDRESS (HEX)	NAME	DESCRIPTION	TYPE	NOTE
0	00	CH_SEL[7:0]	Channel Select	R/W	Ch0:8'b01, Ch1:8'b02, Ch2:8'b04, Ch3:8'b08
1	01	CH0_AMP[7:0]	Channel 0 Current Amplitude	R/W	8-bit DAC programmable
2	02	CH0_PW[7:0]	Channel 0 sink Pulse Width	R/W	
3	03	CH0_DZ0[7:0]	Channel 0 Dead Zone between sink and source pulses; and after source pulse	R/W	
4	04	CH0_DELTA[7:0]	Channel 0 Recharge Width adjustment	R/W	Can be +/-
5	05	CH0_DZ1[7:0]	Channel 0 Dead Zone between sink/source periods	R/W	
6	06	CH0_M[7:0]	Channel 0 number of consecutive sink/source periods	R/W	
7	07	CH0_DZ2[7:0]	Channel 0 Dead Zone between sets of sink/source periods	R/W	
8	08	CH0_THP_DEL[7:0]	Channel 0 Therapy Delay from start of therapy to first stimulus delivered	R/W	
9	09	CH0_N[7:0]	Channel 0 Number of therapy pulses	R/W	
10	0A	CH0_DZ3[7:0]	Channel 0 Dead Zone between therapy pulse sets	R/W	
11	0B	CH0_P[7:0]	Channel 0 Number of master pulses	R/W	
12	0C	CH1_AMP[7:0]	Channel 1 Current Amplitude	R/W	8-bit DAC programmable
13	0D	CH1_PW[7:0]	Channel 1 sink Pulse Width	R/W	
14	0E	CH1_DZ0[7:0]	Channel 1 Dead Zone between sink and source pulses; and after source pulse	R/W	
15	0F	CH1_DELTA[7:0]	Channel 1 Recharge Width adjustment	R/W	Can be +/-
16	10	CH1_DZ1[7:0]	Channel 1 Dead Zone between sink/source periods	R/W	
17	11	CH1_M[7:0]	Channel 1 number of consecutive sink/source periods	R/W	
18	12	CH1_DZ2[7:0]	Channel 1 Dead Zone between sets of sink/source periods	R/W	
19	13	CH1_THP_DEL[7:0]	Channel 1 Therapy Delay from start of therapy to first stimulus delivered	R/W	
20	14	CH1_N[7:0]	Channel 1 Number of therapy pulses	R/W	
21	15	CH1_DZ3[7:0]	Channel 1 Dead Zone between therapy pulse sets	R/W	

22	16	CH1_P[7:0]	Channel 1 Number of master pulses	R/W	
23	17	CH2_AMP[7:0]	Channel 2 Current Amplitude	R/W	8-bit DAC programmable
24	18	CH2_PW[7:0]	Channel 2 sink Pulse Width	R/W	
25	19	CH2_DZ0[7:0]	Channel 2 Dead Zone between sink and source pulses; and after source pulse	R/W	
26	1A	CH2_DELTA[7:0]	Channel 2 Recharge Width adjustment	R/W	Can be +/-
27	1B	CH2_DZ1[7:0]	Channel 2 Dead Zone between sink/source periods	R/W	
28	1C	CH2_M[7:0]	Channel 2 Number of consecutive sink/source periods	R/W	
29	1D	CH2_DZ2[7:0]	Channel 2 Dead Zone between sets of sink/source periods	R/W	
30	1E	CH2_THP_DEL[7:0]	Channel 2 Therapy Delay from start of therapy to first stimulus delivered	R/W	
31	1F	CH2_N[7:0]	Channel 2 Number of therapy pulses	R/W	
32	20	CH2_DZ3[7:0]	Channel 2 Dead Zone between therapy pulse sets	R/W	
33	21	CH2_P[7:0]	Channel 2 Number of master pulses	R/W	
34	22	CH3_AMP[7:0]	Channel 3 Current Amplitude	R/W	8-bit DAC programmable
35	23	CH3_PW[7:0]	Channel 3 sink Pulse Width	R/W	
36	24	CH3_DZ0[7:0]	Channel 3 Dead Zone between sink and source pulses; and after source pulse	R/W	
37	25	CH3_DELTA[7:0]	Channel 3 Recharge Width adjustment	R/W	Can be +/-
38	26	CH3_DZ1[7:0]	Channel 3 Dead Zone between sink/source periods	R/W	
39	27	CH3_M[7:0]	Channel 3 Number of consecutive sink/source periods	R/W	
40	28	CH3_DZ2[7:0]	Channel 3 Dead Zone between sets of sink/source periods	R/W	
41	29	CH3_THP_DEL[7:0]	Channel 3 Therapy Delay from start of therapy to first stimulus delivered	R/W	
42	2A	CH3_N[7:0]	Channel 3 Number of therapy pulses	R/W	
43	2B	CH3_DZ3[7:0]	Channel 3 Dead Zone between therapy pulse sets	R/W	
44	2C	CH3_P[7:0]	Channel 3 Number of master pulses	R/W	
45	2D	RMP_SEL[7:0]	Amplitude ramp selection option for each channel	R/W	Ch0:RMP_SEL[0] Ch1: RMP_SEL[1] Ch2: RMP_SEL[2] Ch3: RMP_SEL[3]
46	2E	BOOST_EN[7:0]	For operation in 6mA current region	R/W	Ch0:BOOST_EN[0] Ch1:BOOST_EN[1]

					Ch2:BOOST_EN[2] Ch3:BOOST_EN[3]
47	2F	PDN[7:0]	Power down register	R/W	PDN=01: Normal operation, PDN=00 System power down
48	30	TRIG[7:0]	The trigger register to start the pulse generation	R/W	The pulses generated when TRIG = AA
49	31	CH_TEST[7:0]	Test mode register for testing different current outputs	R/W	
50	32	GPREG13	General Purpose Register	R/W	No function
51	33	GPREG12	General Purpose Register	R/W	No function
52	34	GPREG11	General Purpose Register	R/W	No function
53	35	GPREG10	General Purpose Register	R/W	No function
54	36	GPREG9	General Purpose Register	R/W	No function
55	37	GPREG8	General Purpose Register	R/W	No function
56	38	GPREG7	General Purpose Register	R/W	No function
57	39	GPREG6	General Purpose Register	R/W	No function
58	3A	GPREG5	General Purpose Register	R/W	No function
59	3B	GPREG4	General Purpose Register	R/W	No function
60	3C	GPREG3	General Purpose Register	R/W	No function
61	3D	GPREG2	General Purpose Register	R/W	No function
62	3E	ASIC_STAT[7:0]	Channel Status Bits corresponding to CH3, CH2, CH1 and CH0	R	Read only, Ch0 -ASIC_STAT[0] Ch1 -ASIC_STAT[1] Ch2 -ASIC_STAT[2] Ch3 -ASIC_STAT[3]
63	3F	ASIC_REV[7:0]	ASIC Design Revision	R	Read only

PACKAGE DIAGRAM

The CSI021 IC is assembled in a 20-lead Quad Flat No-lead package [QFN20]. The package dimensions (in mm) are as shown in the following package drawing.